REMARKS/ARGUMENTS

Claims 1-20 are pending in the present application. With this amendment, claims 2-3, 8-9, and 19 have been canceled; claims 1, 7, and 15 have been amended. Reconsideration of the claims is respectfully requested.

I. Claim Amendments

Claim 1 has been amended to incorporate the features of claims 2-3; claim 7 has been amended to incorporate the features of claims 8-9; claim 15 has been amended to incorporate the features of claim 19. The independent claims have been amended by adding the features of pending dependent claims. Therefore, the scope of the claims has not changed.

II. 35 U.S.C. § 103, Obviousness

II.A. Claims 1-5, 7-13 and 15-20 over *Arndt* in view of *Stine*

The Examiner has rejected claims 1-5, 7-13 and 15-20 under 35 U.S.C. § 103(a) as being unpatentable over *Arndt*, Logical Partitioning Via Hypervisor Mediated Address Translation, U.S. Patent No. 6,877,158, dated April 5, 2005 (hereinafter referred to as "*Arndt*") in view of *Stine* et al., Memory Allocation System, U.S. Patent No. 6,629,111, dated September 30, 2003 (hereinafter referred to as "*Stine*"). This rejection is respectfully traversed.

The Examiner states:

> **As per claims 1,7, 15 and 20**, Arndt discloses "a method of supporting memory addresses with holes, the method comprising the computer implemented steps of: virtualizing a first physical address range allocated for system memory for, an operating system run by a processor configured to support logical partitioning to produce a first logical address range; virtualizing a second physical address range allocated for system memory for the operating system to produce a second logical address range, wherein the first physical address range and the second physical address range are non-contiguous and the first logical address range and the second logical address range are contiguous" as **["methods and systems for managing** resources among multiple operating system images within a logically partitioned operating system" (Column 1, lines 1-13) wherein different ***110*** adapters are assigned to different partitions (Column 3, lines 3-16) and explains having discontinuous physical memory for .these continuous logical partitions (Column 5, line 59-Column 6, line 19). Please also note (Columns 9, line 36 - Column 10, line 35)].
> Arndt does not disclose expressly "virtualizing a memory mapped input/output physical address range that is intermediate the first physical address range and the second physical address range to produce a third logical address range, wherein a lowermost logical address of the third logical address range exceeds a respective uppermost logical address of the first and second logical address ranges."

Stine discloses "virtualizing a memory mapped input/output physical address range that is intermediate the first physical address range and the second physical address range to produce a third logical address range, wherein a lowermost logical address of the third logical address t range exceeds a respective uppermost logical address of the first and second logical address ranges" as ["a memory allocation scheme which may be used to conserve memory that is to be accessed by one or more clients (e.g. computers or applications)" (Column 5, lines 5-8) and explains identifying regions of memory which may normally go unused "memory holes" and allocating these regions to clients (Column 3, lines 8-56, Figure 10 and Column 10, lines 9-51) and explains that "once mapped to a particular file, the entry may store information associated with that particular file, such as the name of the file, the size of the file, and the hole size defining an unallocated portion of the memory segment once the file has been stored in the memory segment" (Column 3, line 57-Column 5, line 5) wherein memory is 'mapped using a TLB (Column 5, lines 6-24)].
Arndt (US 6,877,158) and Stine ct al. (US 6,629,11 I) are analogous art because they are from the same field of endeavor of computer memory access and control.
At the time of the invention it would have been obvious to a person of ordinary skill in the art modify the logically partitioned virtualization system wherein a non-contiguous physical address range is virtualized into a contiguous virtual address range as taught by Arndt and map memory access operations within memory holes as taught by Stine.
The motivation for doing so would have been because Stine discloses that allocating "memory holes" to processes or applications allows [the conservation of physical memory as "the corresponding number of pages required in virtual memory are minimized;" also facilitating the utilization of memory as "when a hole in a memory segment already containing data is used, a new TLB entry need not be created since the hole is mapped in an entry in the memory segment list" (Column 4, lines 6-24)]. Furthermore Arndt discloses the having a logically partitioned system wherein partitions are assigned to different resources wherein noncontiguous physical memory is assigned to contiguous virtual partitions is desirable as it allows ["fine grain allocation of resources to partitions without necessitating the physical movement of the hardware during configuration" (Column **1,** line 66-Column **2,** line **3)J.**
Therefore, it would have been obvious to combine Stine et al. (US 6,629,111) with Arndt (US 6,877,158) for the benefit of creating a memory virtualization system to obtain the invention as specified in claims I , 7, 15 and 20.
As per claims 2,8-11 and 16-19, the combination of Arndt and Stine discloses the method/program/system of claims 1, 7 and 15 [See rejection to claims 1,7 and 15 above] ' wherein "the steps of virtualizing the first physical address range, the second physical address range, and the memory mapped input/output physical address range comprises maintaining a mapping table that defines physical addresses and corresponding logical addresses" [With respect to this limitation, Arndt discloses having a page frame table per OS image wherein different OS images are assigned to different logical partitions and a "hypervisor 310" for performing virtualization having "allocation table.380" (Column 5, lines 37-49; Figure 3; Column 3, lines 3-16). Furthermore, Stine discloses virtualization using a "TLB" (Figure ***6.***
As per claim 3, the combination of Arndt and Stine discloses the method program of claim 2, [See rejection to claim 2 above] "wherein maintaining the

> mapping table further comprises maintaining the mapping table in a physical address space allocated to one of the first and second physical address ranges, and wherein the physical address space is unavailable to an operating system accessing the first and second physical address ranges" [Arndt discloses this concept as a "hypervisor 210" having allocation table 380 which controls platform's 200 virtual address translation hardware 280 (Column 4, line 58-Column 5, line 30; Figures **2**-3).

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Applicant's claim 1 now includes the features of claims 2 and 3. Claim 1 now recites "wherein maintaining the mapping table further comprises maintaining the mapping table in a physical address space allocated to one of the first and second physical address ranges, and wherein the physical address space is unavailable to an operating system accessing the first and second physical address ranges." Thus, in order to render Applicant's claim obvious, the combination of *Arndt* and *Stine* must teach wherein the physical address space is unavailable to an operating system accessing the first and second physical address ranges. The combination does not teach or suggest this feature.

According to Applicant's claims, the physical address space is allocated to one of the first and second physical address ranges. Applicants understand the Examiner to believe the physical resources 360 are analogous to the physical address ranges claimed by Applicants. If the physical resources 360 are indeed analogous to the physical address ranges claimed by Applicants, then there must be a physical address space that is allocated to one of the physical resources 360. Further, the physical address space must be unavailable to an operating system that is accessing the physical resource 360. *Arndt* does not teach this.

Arndt teaches page frame tables 320-350 containing mappings for virtual pages for an operating system image to a page frame 361-371. *Arndt* does not teach a physical address space in physical resources 360 as being unavailable to an operating system that is accessing physical resources 360. Because *Arndt* does not teach this feature, the combination of *Arndt* and *Stine* does not render Applicants claims obvious.

In order to render Applicant's claim obvious, the combination of *Arndt* and *Stine* must also teach the mapping table being maintained in a physical address space that is allocated to one of the first and second physical address ranges. The Examiner appears to believe the physical resources 360 taught by *Arndt* are analogous to the physical address ranges claimed by Applicants. Assuming, for the sake of argument, that this is indeed the case, the allocation table 380, believed by the Examiner to be analogous to the mapping table claimed by Applicants, must be maintained in a physical address space that is allocated to one of the physical resources 360. This is not taught by *Arndt*, however.

The allocation table 380 is depicted in Figure 3 as being separate from physical resources 360. Allocation table 380 is not maintained within physical resources 360. Therefore, allocation table 360 is

not maintained within a physical address space that is allocated to one of the physical resources 360. Thus, *Arndt* does not teach this feature of Applicant's claim 1. Because *Arndt* does not teach this feature of Applicant's claim 1, the combination of *Arndt* and *Stine* does not render Applicant's claim 1 obvious.

Applicant has also amended claim 7 to include the features of claim 8-9. Claim 7 now recites: "instructions for maintaining a mapping table that defines physical addresses and their corresponding logical addresses; and wherein the mapping table is maintained in at least one of the first range of contiguous physical addresses and the second range of contiguous physical addresses".

As discussed above, *Arndt* does not teach maintaining the allocation table 380 in one of the physical resources 360. Therefore, *Arndt* does not teach wherein the mapping table is maintained in at least one of the first range of contiguous physical addresses and the second range of contiguous physical addresses. Thus, the combination of *Arndt* and *Stine* does not render Applicant's claim 7 obvious.

Applicant has amended claim 15 to include the features of claim 19. Claim 15 now recites: "a set of instructions that is executed by the processor for virtualizing the first, second, and third ranges of contiguous physical addresses, wherein the set of instructions is maintained in the memory in at least one of the first and second ranges of contiguous physical addresses".

As discussed above, *Arndt* does not teach maintaining the allocation table 380 in one of the physical resources 360. Therefore, *Arndt* does not teach wherein the set of instructions is maintained in the memory in at least one of the first and second ranges of contiguous physical addresses. Thus, the combination of *Arndt* and *Stine* does not render Applicant's claim 15 obvious.

The remaining claims depend from one of the independent claims discussed above and are patentable for the reasons given above. Therefore, the rejection of claims 1-5, 7-13 and 15-20 under 35 U.S.C. § 103(a) has been overcome.

II.B. Claims 6 and 14 over *Arndt* in view of *Stine* and further in view of *Yazdy*

The Examiner has rejected claims 6 and 14 under 35 U.S.C. § 103(a) as being unpatentable over *Arndt* in view of *Stine* as applied to claims 1-5 above, and further in view of *Yazdy* et al., Cache Management During Cache Inhibited Transactions for Increasing Cache Efficiency, U.S. Patent No. 6,256,710, dated July 3, 2001 (hereinafter referred to as "*Yazdy*"). This rejection is respectfully traversed.

Claim 6 depends from claim 1. Applicant's claim 6 recites: "wherein the memory mapped input/output physical address range is allocated for cache inhibited addresses".

Claim 14 depends from claim 7. Applicant's claim 14 recites: "wherein the third range of contiguous physical addresses is allocated for cache inhibited memory mapped input/output addresses".

The Examiner states that the combination of *Arndt* and *Stine* does not teach the physical addresses being allocated for cache inhibited memory mapped input/output addresses. The Examiner relies on *Yazdy* to teach this feature.

Yazdy teaches an area of main memory that is non-cacheable. See *Yazdy*, column 2, lines 23-14.

Yazdy does not, however, teach maintaining the mapping table in a physical address space allocated to one of the first and second physical address ranges, or and wherein the physical address space is unavailable to an operating system accessing the first and second physical address ranges. Therefore, the combination of *Arndt*, *Stine*, and *Yazdy* does not render Applicant's claim 6 obvious.

Yazdy does not teach wherein the set of instructions is maintained in the memory in at least one of the first and second ranges of contiguous physical addresses. Therefore, the combination of *Arndt*, *Stine*, and *Yazdy* does not render Applicant's claim 14 obvious.

III. Conclusion

It is respectfully urged that the subject application is patentable over *Arndt, Stine* and *Yazdy* and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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